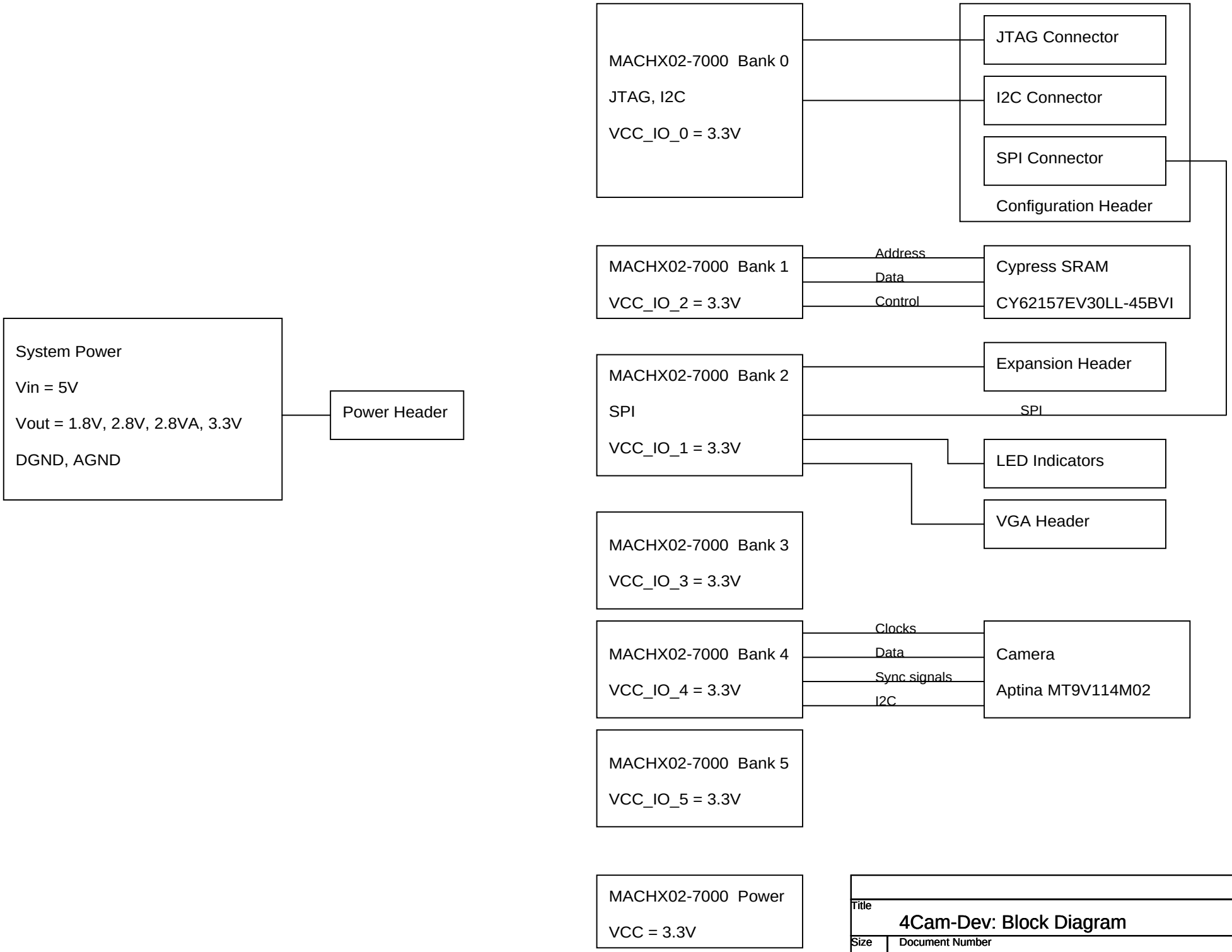

Title	4Cam-Dev: Block Diagram	
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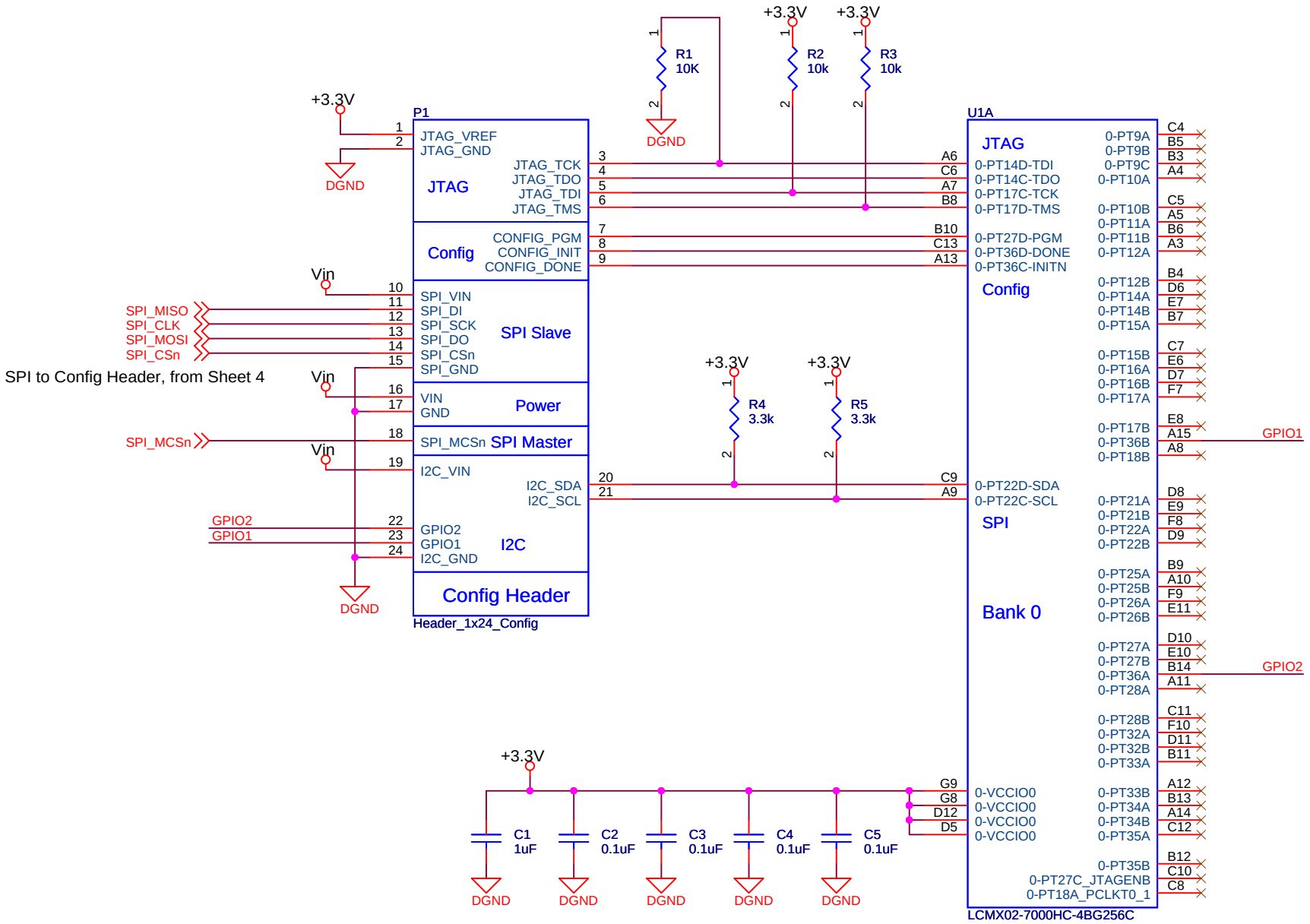

Title	4Cam-Dev: Configuration Header	
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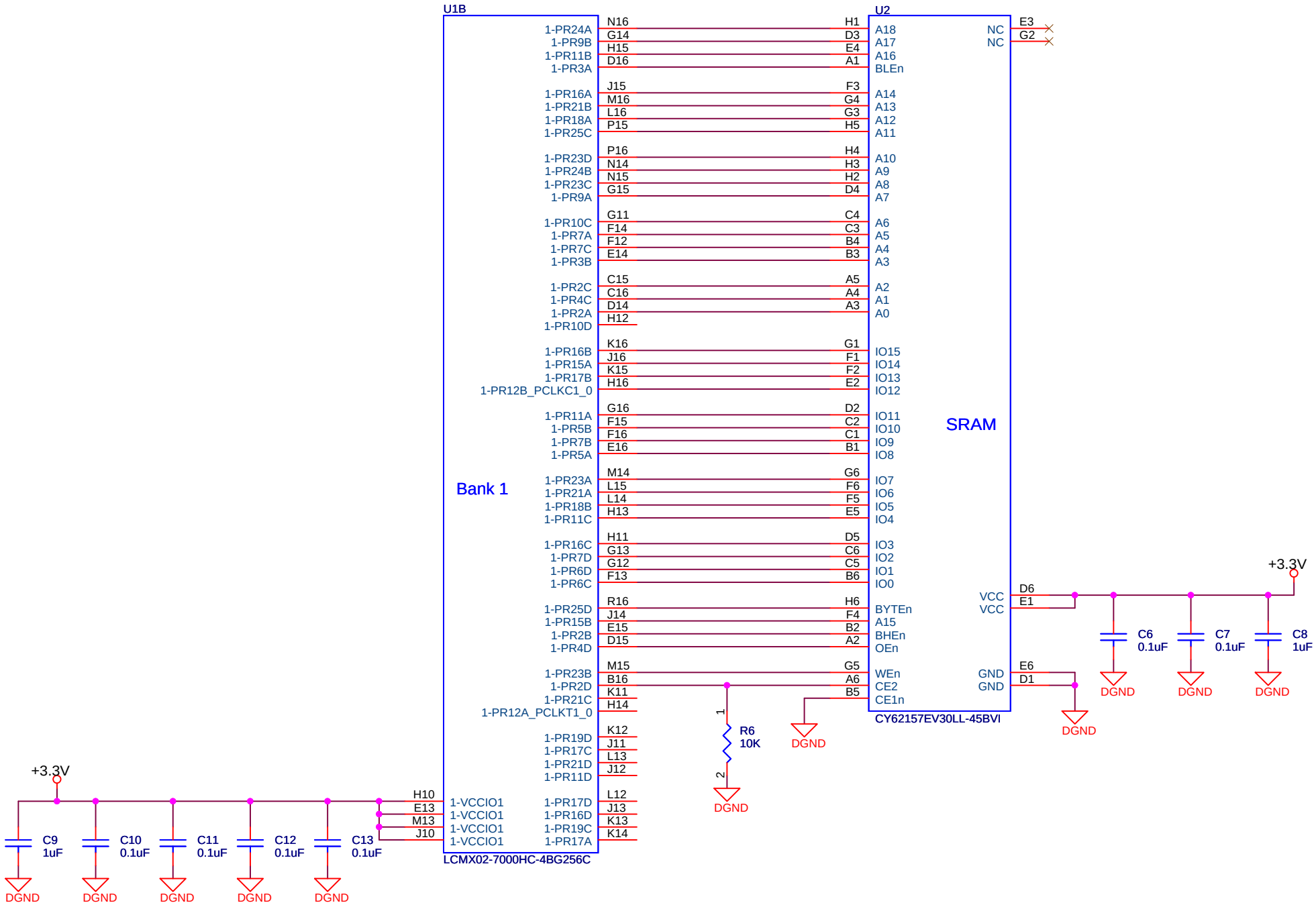

Title	4Cam-Dev: SRAM	
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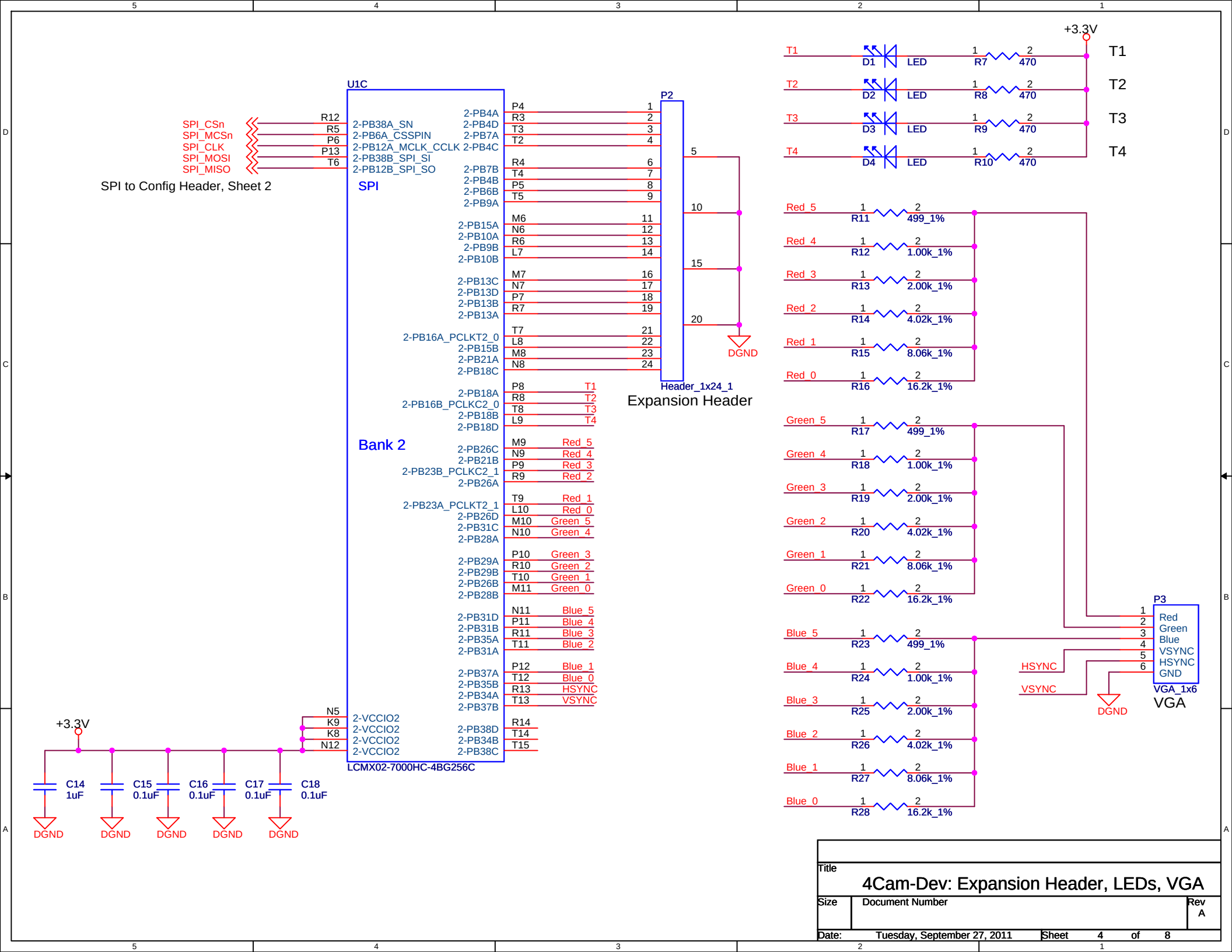
U1C
SPI_CSn
SPI_MCSn
SPI_CLK
SPI_MOSI
SPI_MISO
SPI to Config Header, Sheet 2
R12
R5
P6
P13
T6
2-PB38A_SN
2-PB6A_CSSPIN
2-PB12A_MCLK_CCLK
2-PB38B_SPI_SI
2-PB12B_SPI_SO
SPI
2-PB4A
2-PB4D
2-PB7A
2-PB4C
2-PB7B
2-PB4B
2-PB6B
2-PB9A
2-PB15A
2-PB10A
2-PB9B
2-PB10B
2-PB13C
2-PB13D
2-PB13B
2-PB13A
2-PB16A_PCLKT2_0
2-PB15B
2-PB21A
2-PB18C
2-PB18A
2-PB16B_PCLKC2_0
2-PB18B
2-PB18D
Bank 2
2-PB26C
2-PB21B
2-PB23B_PCLKC2_1
2-PB26A
2-PB23A_PCLKT2_1
2-PB26D
2-PB31C
2-PB28A
2-PB29A
2-PB29B
2-PB26B
2-PB28B
2-PB31D
2-PB31B
2-PB35A
2-PB31A
2-PB37A
2-PB35B
2-PB34A
2-PB37B
2-PB38D
2-PB34B
2-PB38C
P4
R3
T3
T2
R4
T4
P5
P6
T5
M6
N6
R6
L7
M7
N7
P7
R7
T7
L8
M8
N8
P8
R8
T8
L9
M9
N9
P9
R9
T9
L10
M10
N10
P10
R10
T10
M11
N11
P11
R11
T11
P12
T12
R13
T13
R14
T14
T15
N5
K9
K8
N12
2-VCCIO2
LCMX02-7000HC-4BG256C
P2
Header_1x24_1
Expansion Header
DGND
T1
T2
T3
T4
Red_5
Red_4
Red_3
Red_2
Red_1
Red_0
Green_5
Green_4
Green_3
Green_2
Green_1
Green_0
Blue_5
Blue_4
Blue_3
Blue_2
Blue_1
Blue_0
HSYNC
VSYNC
+3.3V
D1
D2
D3
D4
LED
R7
R8
R9
R10
470
R11
R12
R13
R14
R15
R16
R17
R18
R19
R20
R21
R22
R23
R24
R25
R26
R27
R28
499_1%
1.00k_1%
2.00k_1%
4.02k_1%
8.06k_1%
16.2k_1%
P3
Red
Green
Blue
VSYNC
HSYNC
GND
VGA_1x6
VGA
C14
1uF
C15
0.1uF
C16
0.1uF
C17
0.1uF
C18
0.1uF
Title
4Cam-Dev: Expansion Header, LEDs, VGA
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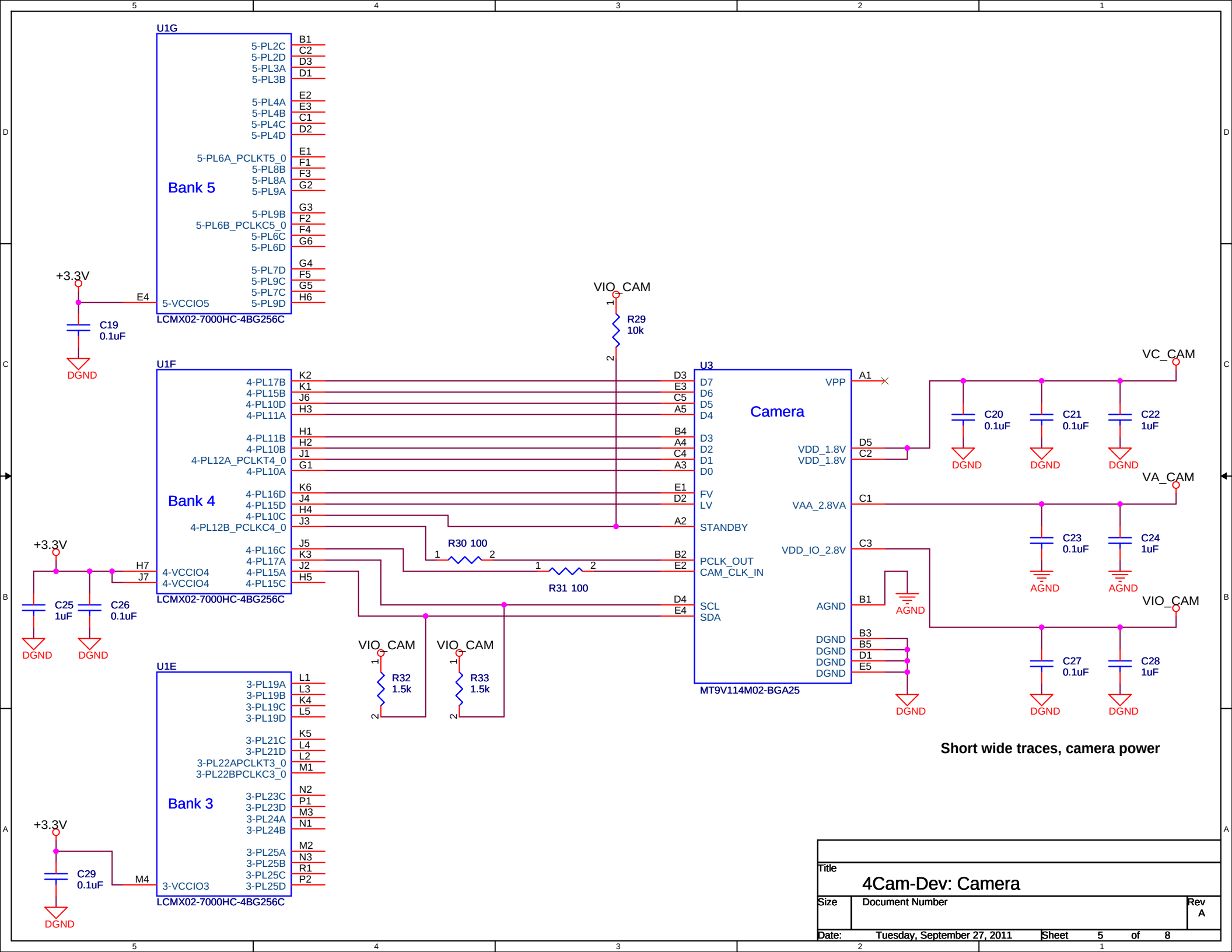
U1G
Bank 5
LCMX02-7000HC-4BG256C
U1F
Bank 4
LCMX02-7000HC-4BG256C
U1E
Bank 3
LCMX02-7000HC-4BG256C
U3
Camera
MT9V114M02-BGA25
+3.3V
DGND
AGND
VIO_CAM
VC_CAM
VA_CAM
R29 10k
R30 100
R31 100
R32 1.5k
R33 1.5k
C19 0.1uF
C20 0.1uF
C21 0.1uF
C22 1uF
C23 0.1uF
C24 1uF
C25 1uF
C26 0.1uF
C27 0.1uF
C28 1uF
C29 0.1uF
Short wide traces, camera power
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4Cam-Dev: Camera
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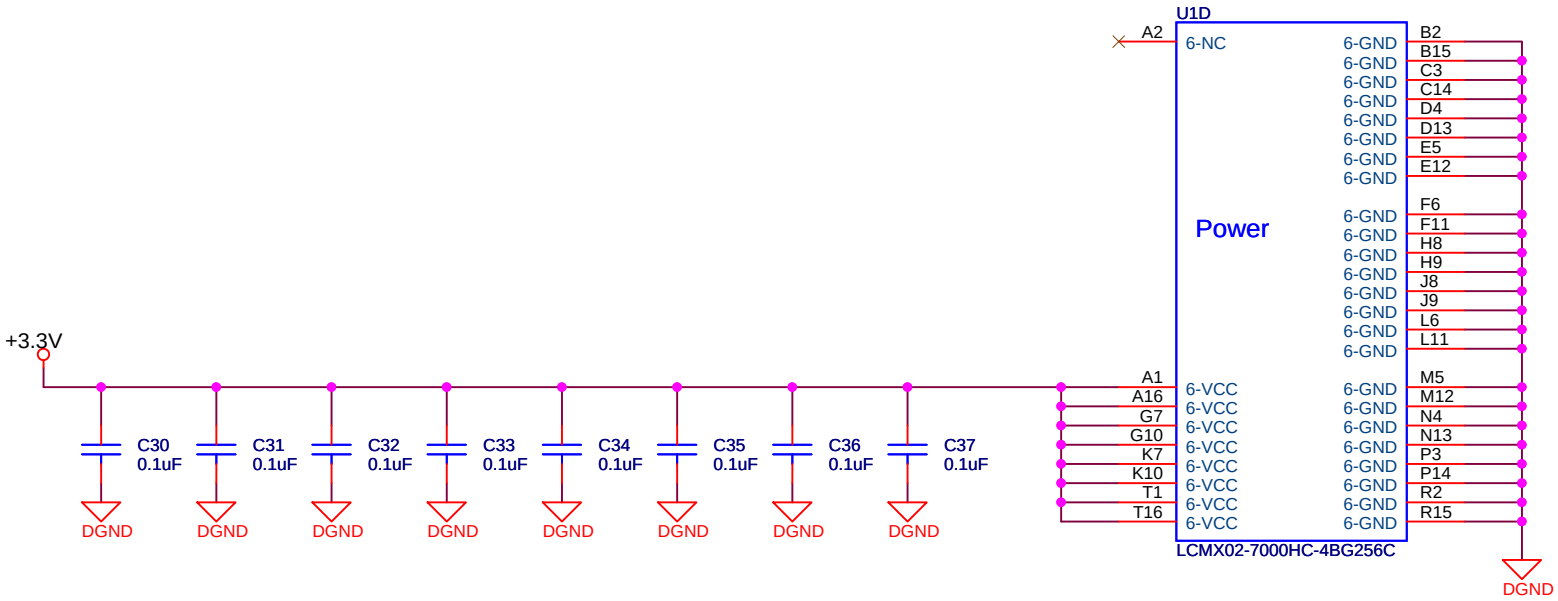

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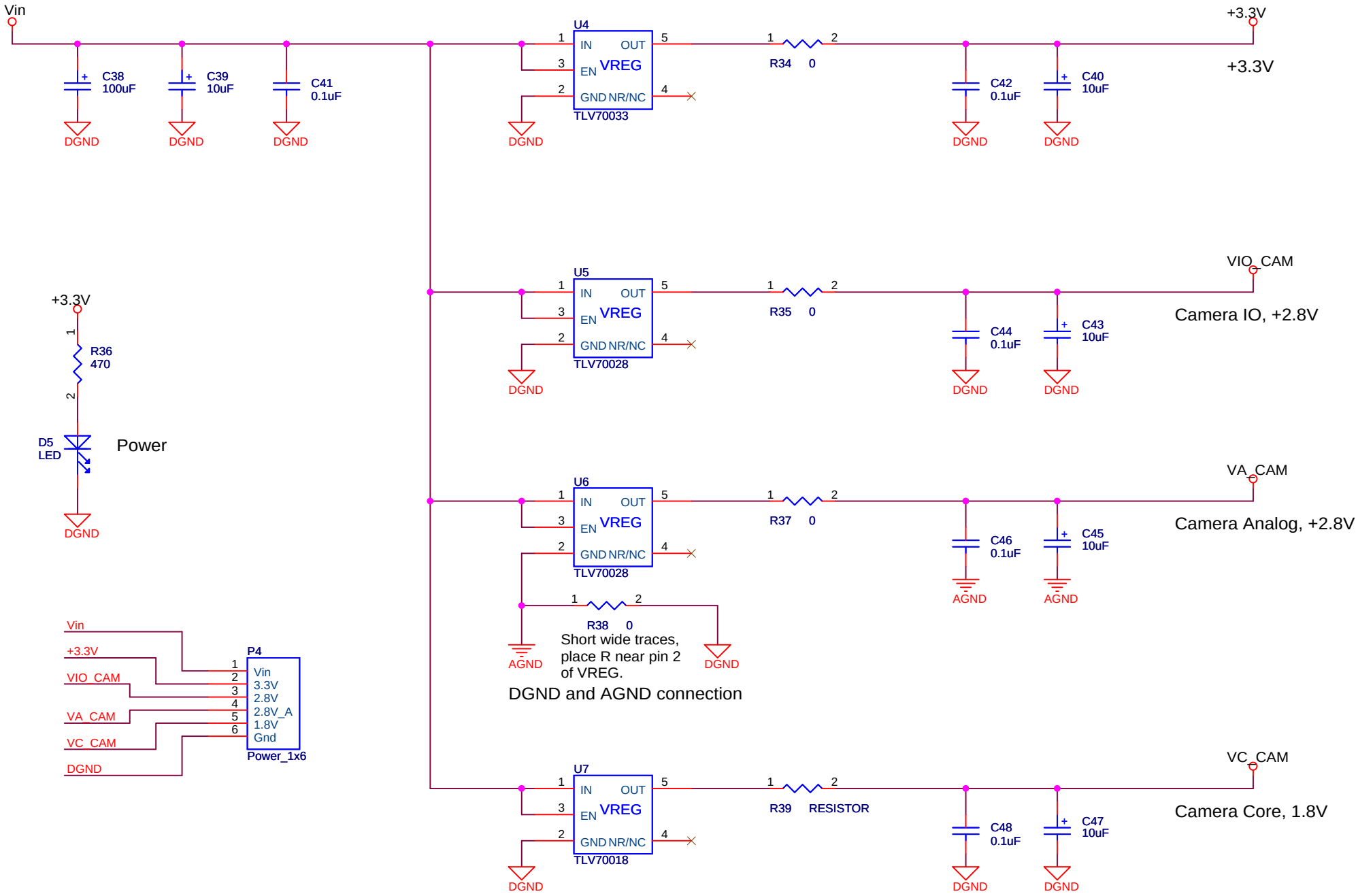

Short wide traces, whole page

Title	4Cam-Dev: Voltage Regulators	
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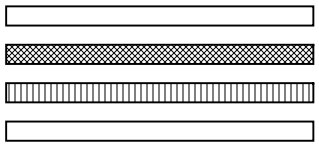
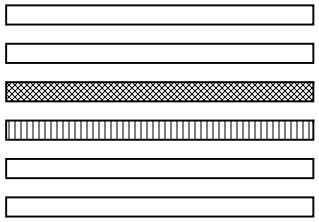
Lattice layout Notes:
1) Keep SRAM data/address traces of equivalent length.
2) Keep camera data traces of equivalent length.
3) Check that the power planes are continuous under the FPGA bank area, with vias down to the planes, no traces.
4) Outside the FPGA area, use greater than minimum clearance between signal vias and GND/power planes so they are not too capacitive, and make the vias small diameter. Directly under the FPGA, the vias can have minimum clearance to power planes, to help reduce SSO (Simutaneous Switching Output noise).
5) Where it makes sense, add external series 33 ohm resistors to fast IO outputs to lower SSO (Simutaneous Switching Output noise) and received signal reflections.
6) Use slow slew settings where possible .
7) Add more caps of various sizes on power supplies, include 0.01uF and 0.001uF, smallest caps directly under the Lattice device. Recommend a minimum of 0.1uF, 0.01uF, and 1000pF ceramic caps per bank from VCCIO to GND, along with a 10uF or higher value.
8) The smaller value caps work best when placed directly under the FPGA at the VCCIO pins served, larger value caps can be further out.
9) This is not a very high speed design, so the 0.001uF caps may not be necessary. Use 0.1uF with a ratio of one cap for each power pin.
10) Small value caps must go directly under CPLD power pins.
11) Power and ground planes should be filled metal areas with no breaks or large cutouts in the planes where:
- signals travel on high speed PCB traces on layers adjacent to the planes
- as well as directly under the FPGA.



Top Layer - trace routing
GND
Power
Bottom Layer - trace routing - bypass caps

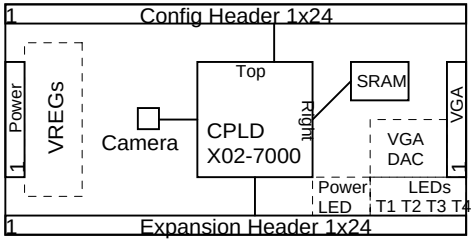
4 PCB Layers



Layer 1 - trace routing
Layer 2 - trace routing
GND
Power
Layer 5 - trace routing
Layer 6 - trace routing - bypass caps

6 PCB Layers

Aptina MT9V114M02-BGA25 Questions
1) Use 3.3V instead of 2.8V?
2) Combine VIO and VAA, use one voltage regulator?
3) Pin D5 in datasheet different from eval board.
4) Pin E5 in datasheet different from eval board.
5) Are input pins 3.3V tolerant?
6) Are input pins 5V tolerant?
7) Which direction is "image up" for the camera package?



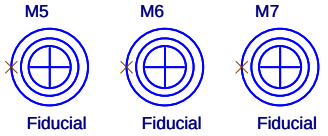
PCB Layout

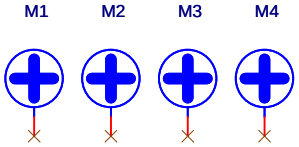
2.4 inch width
1.2 inch height

From Aptina:
1. Standby pin can't float! Tie to ground if they do not want standby mode to be asserted and tie high if they want to assert standby.
2. You should connect per the data sheet E5 to ground.
3. Tie analog and digital grounds together. Could use same ground plane.
4. D5 needs to be connected to 1.8 volts not 2.8 volts.
5. Inputs not 3.3 or 5 volt tolerant.
6. Recommend separate LDO for analog supply otherwise VDD_IO can inject noise in image.

Lattice 256-ball caBGA Breakout and Routing Examples

http://goo.gl/qsPIO





Title	4Cam-Dev: PCB Layout	
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